

### Description

The AP300N10TLG2 uses advanced **APM-SGT<sub>11</sub>** technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 100V$   $I_D = 300A$

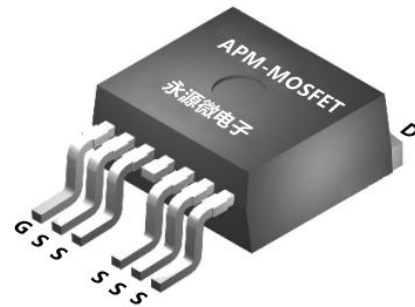
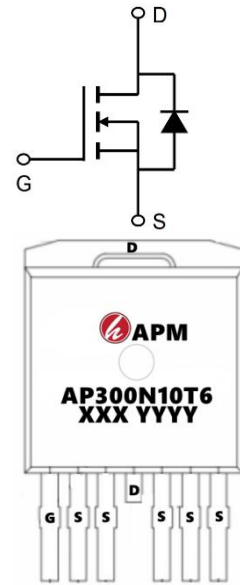
$R_{DS(ON)} < 2.0m\Omega$  @  $V_{GS}=10V$  (Type: **1.6m $\Omega$** )

### Application

DC/DC Converter

LED Backlighting

Power Management Switches



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP300N10T6	TO263-6L	AP300N10T6 XXX YYYYY	800

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	300	A
$I_D @ T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	210	A
IDM	Pulsed Drain Current	960	A
EAS	Single Pulse Avalanche Energy	2340	mJ
IAS	Avalanche Current	53.4	A
$P_D @ T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	313	W
TSTG	Storage Temperature Range	-55 to 175	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 175	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	0.15	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case	40	$^\circ C/W$

## 100V N-Channel Enhancement Mode MOSFET

### Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	100	107	-	V
IGSS	Gate-body Leakage current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
IDSS	Zero Gate Voltage Drain Current T <sub>J</sub> =25°C	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V	-	-	1	μA
	Zero Gate Voltage Drain Current T <sub>J</sub> =100°C		-	-	100	
VGS(th)	Gate-Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.0	3.0	4.0	V
RDS(on)	Drain-Source on-Resistance <sup>4</sup>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 50A	-	1.6	2.0	mΩ
gfs	Forward Transconductance <sup>4</sup>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 50A	-	190	-	S
Ciss	Input Capacitance	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0V, f = 1MHz	-	11300	-	pF
Coss	Output Capacitance		-	1400	-	
Crss	Reverse Transfer Capacitance		-	48	-	
R <sub>g</sub>	Gate Resistance	f = 1MHz	-	2	-	Ω
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 50V, I <sub>D</sub> = 20A	-	165	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	67	-	
Q <sub>gd</sub>	Gate-Drain Charge		-	35	-	
td(on)	Turn-on Delay Time	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 50V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = 20A	-	37	-	ns
t <sub>r</sub>	Rise Time		-	112	-	
td(off)	Turn-off Delay Time		-	85	-	
t <sub>f</sub>	Fall Time		-	115	-	
trr	Body Diode Reverse Recovery Time	I <sub>F</sub> = 30A, dI/dt=500A/μs	-	100	-	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> = 30A, dI/dt=100A/μs	-	323	-	nC
VSD	Diode Forward Voltage <sup>4</sup>	I <sub>S</sub> = 50A, V <sub>GS</sub> = 0V	-	-	1.2	V
IS	Continuous Source Current T <sub>C</sub> =25°C	-	-	-	300	A

#### Notes:

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、 The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=50V, V<sub>GS</sub>=10V, L=0.5mH, I<sub>AS</sub>=50A
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

Typical Characteristics

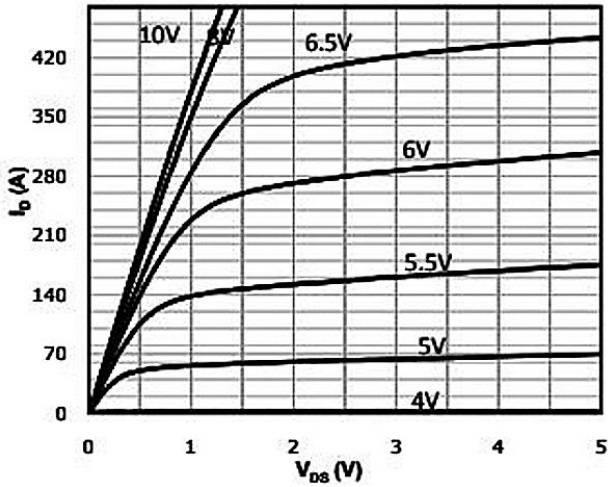


Figure 1. Output Characteristics

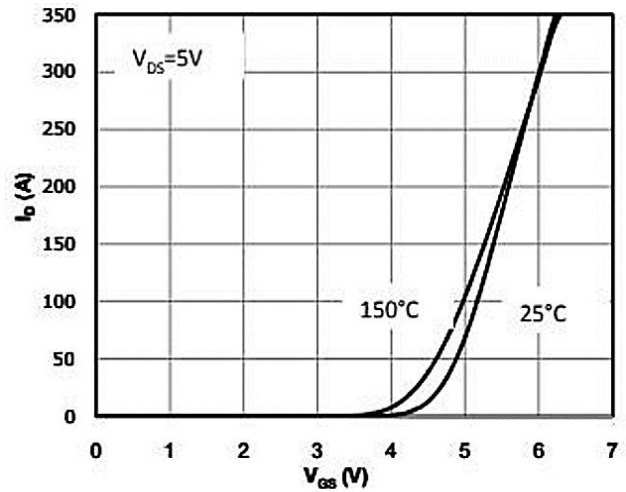


Figure 2. Transfer Characteristics

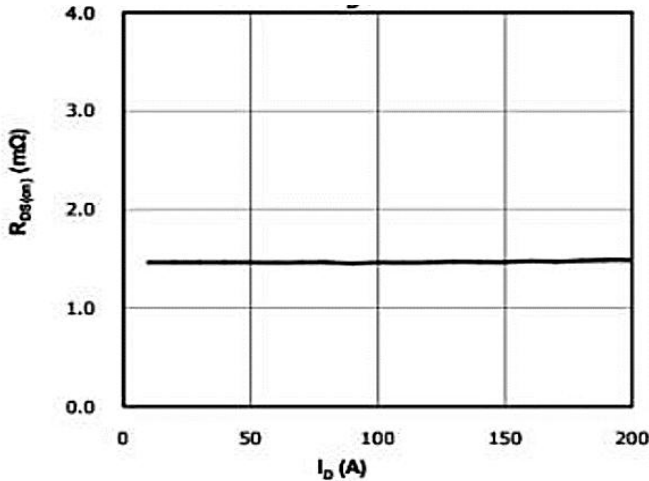


Figure 3. RDS (ON) VS Drain Current and Vgs

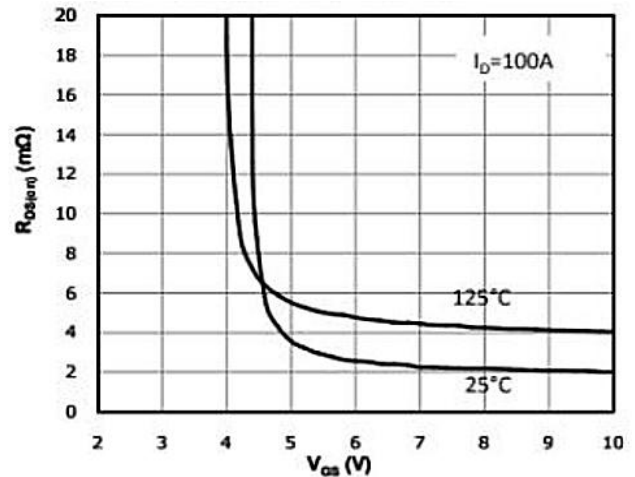


Figure 4. RDS(ON) vs. VGS

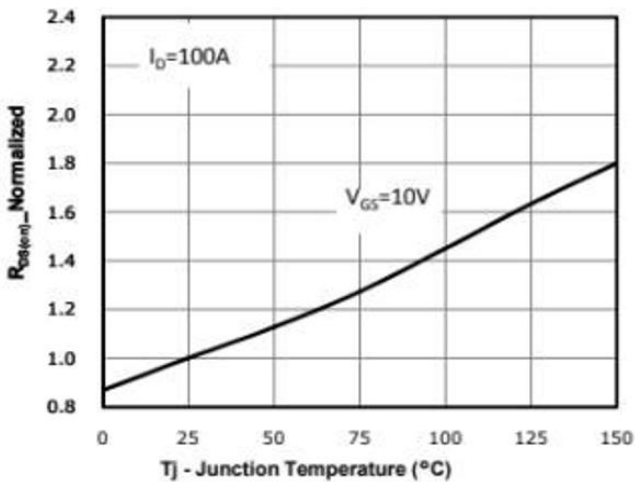


Figure 5. RDS(ON) vs. Temperature

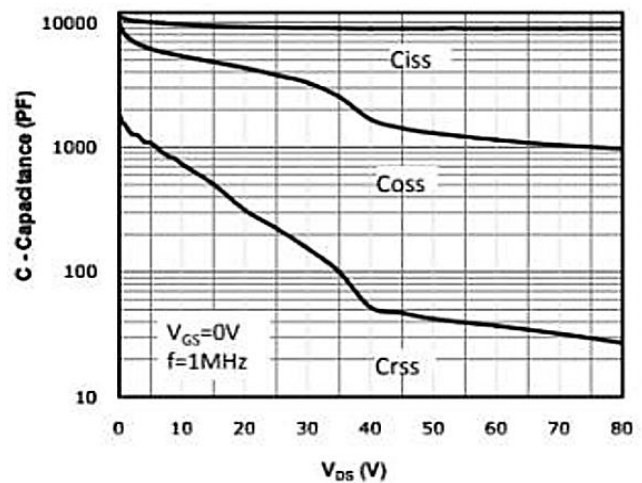


Figure 6. Capacitance Characteristics

## 100V N-Channel Enhancement Mode MOSFET

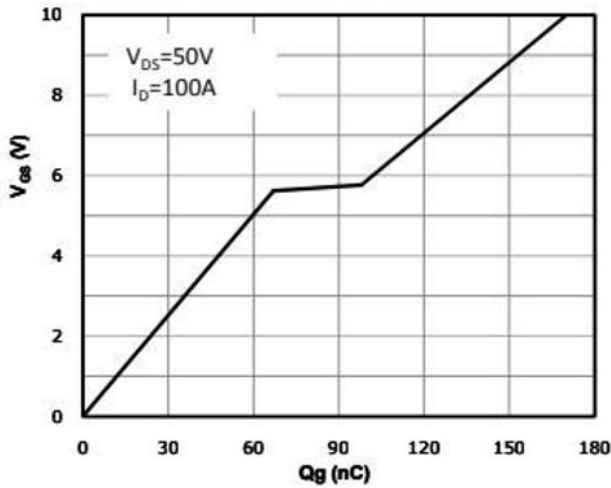


Figure 7. Gate Charge Characteristics

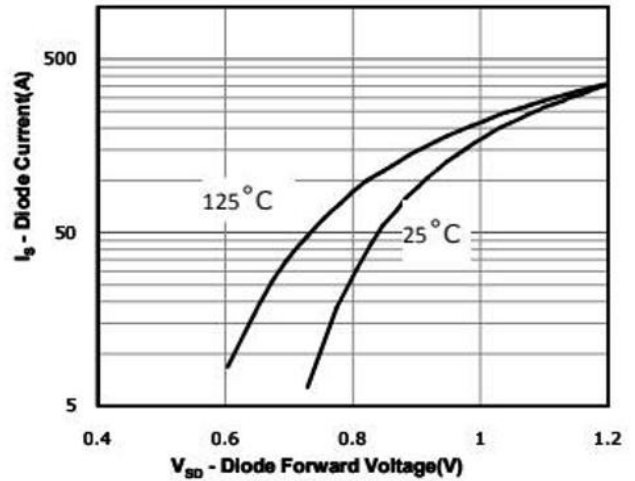


Figure 8. Body-Diode Forward Characteristics

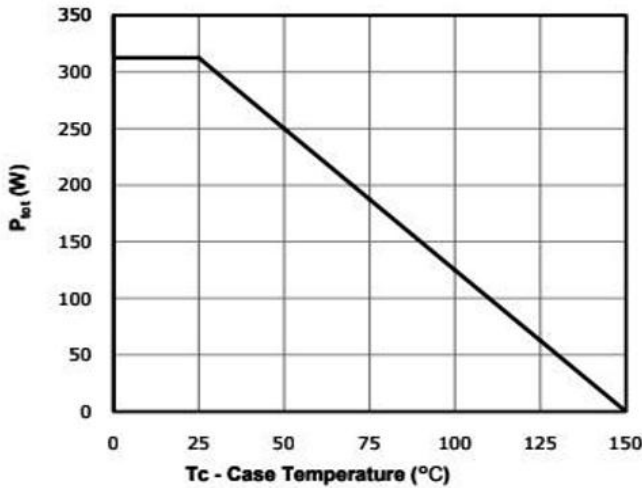


Figure 9. Power Dissipation

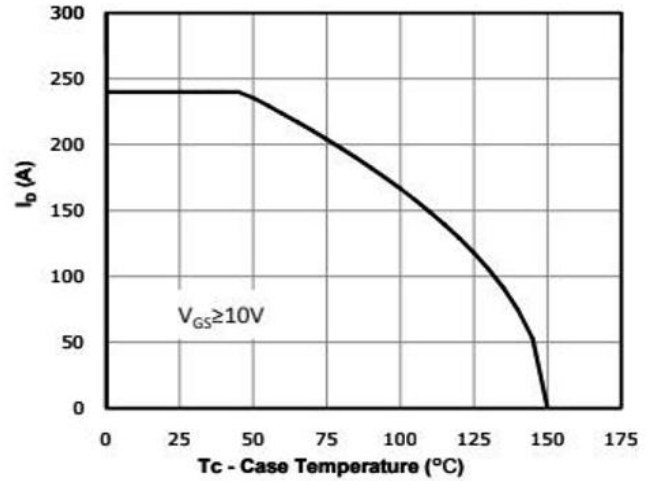


Figure 10. Drain Current Dearing

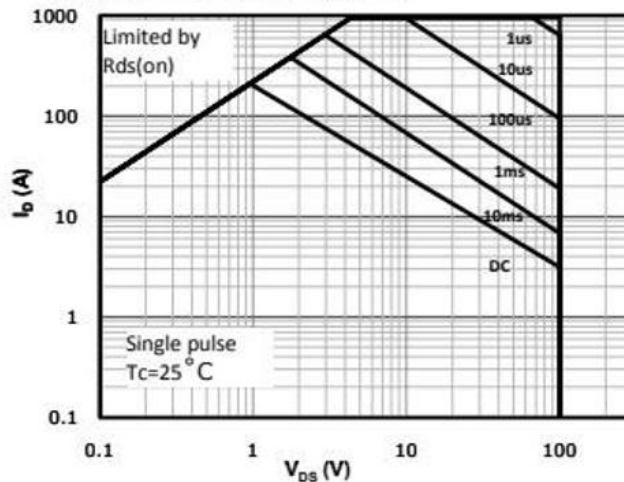
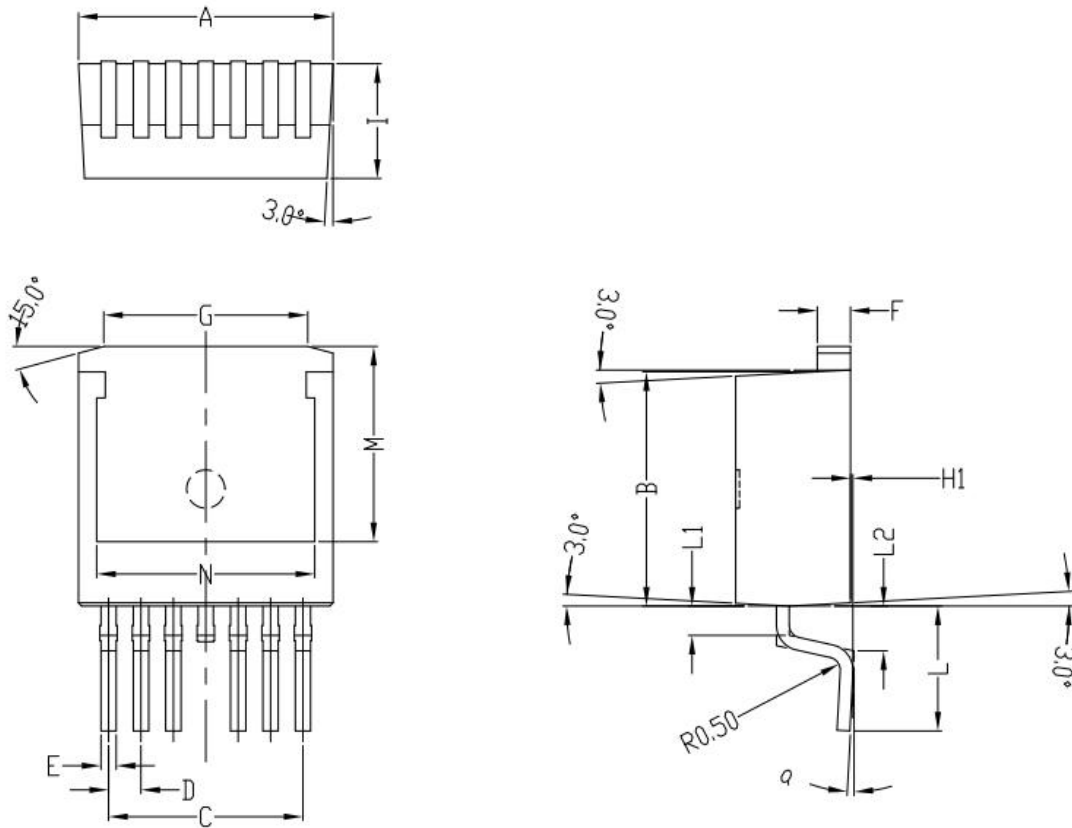


Figure 11. Safe Operating Area

### Package Mechanical Data-TO263-6L-SLK



Symbol	Common		
	mm		
	Mim	Nom	Max
A	9.88	9.98	10.08
B	9.09	9.19	9.29
C	7.54	7.62	7.70
D	1.23	1.27	1.31
E	0.55	0.6	0.65
F	1.27	1.30	1.33
G	7.7	8	8.3
H1	-0.1	+0.10	+0.2
I	4.42	4.50	4.58
L	4.60	4.90	5.20
L1	1.05	1.15	1.25
L2	1.66	1.76	1.86
a	-7°	0°	7°
N	8.25	8.55	8.85
M	7.36	7.66	7.96

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Edition	Date	Change
Rve1.0	2022/5/5	Initial release

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